



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN THE APPLICATION OF:

**WILLIAM J. BORLAND ET AL.**

CASE NO.: **EL0497 US NA**

APPLICATION NO.: **10/725,888**

CONFIRMATION NO.:

GROUP ART UNIT:

EXAMINER:

FILED: **DECEMBER 2, 2003**

FOR: **PRINTED WIRING BOARDS HAVING CAPACITORS AND METHODS OF MAKING THEREOF**

### INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

In compliance with 37 CFR 1.97 and 1.98, Applicants would like to bring to the attention of the U.S. Patent and Trademark Office information that may be helpful in the examination of the above-identified patent application. All of the information is listed on an attached Forms PTO/SB/08.

Should any fee be required in connection with the filing of this Information Disclosure Statement, please charge such fee to Deposit Account No. 04-1928 (E. I. du Pont de Nemours and Company).

Respectfully submitted,

**REBECCA W. TULLOCH**  
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Dated: 2/23/2004

Enclosures

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Sheet	1	of	4
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**Complete if Known**

Application Number	10/725,888
Filing Date	December 2, 2003
First Named Inventor	William J. Borland
Art Unit	
Examiner Name	
Attorney Docket Number	EL0497 US NA

## U. S. PATENT DOCUMENTS

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## FOREIGN PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T <sup>6</sup>
		Country Code <sup>3</sup> Number <sup>4</sup> Kind Code <sup>5</sup> (if known)	MM-DD-YYYY			
		JP 2003-92460	05-31-2002			
		JP 2-153589	06-13-1990	Ibiden KK		
		JP 2001-168491	12-09-1999			

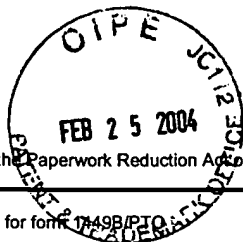
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**Complete if Known**

Application Number

10/725,888

Filing Date

December 2, 2003

First Named Inventor

William J. Borland

Art Unit

Examiner Name

Attorney Docket Number

EL0497 US NA

**NON PATENT LITERATURE DOCUMENTS**

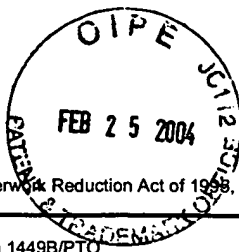
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		JOHN FELTEN AND SAUL FERGUSON, Embedded Ceramic Resistors and Capacitors for PWB, IP Printed Circuit Expo, San Diego, CA, April 2000.	<input type="checkbox"/>
		JOHN J. FELTEN AND SAUL FERGUSON, Ceramic Resistors and Capacitors Embedded in PWB, IPC, San Diego, April 5, 2000.	<input type="checkbox"/>
		JOHN J. FELTEN AND SAUL FERGUSON, Ceramic Resistors and Capacitors Embedded in PWB, IMAPS, Denver, April 29, 2000.	<input type="checkbox"/>
		JOHN J. FELTEN AND WILLIAM J. BORLAND, Embedded Ceramic Passives in PWB: Process Development, IPC Printed Circuit Expo, Anaheim, CA, April 2001.	<input type="checkbox"/>
		JOHN J. FELTEN AND WILLIAM J. BORLAND, Ceramic Resistors and Capacitors Embedded in PWB's, IPC Expo, April 3, 2001.	<input type="checkbox"/>
		WILLIAM BORLAND, Designing for Embedded Passives, Printed Circuit Design, August 2001.	<input type="checkbox"/>

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Sheet

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4

**Complete if Known**

Application Number

10/725,888

Filing Date

December 2, 2003

First Named Inventor

William J. Borland

Art Unit

Examiner Name

Attorney Docket Number

EL0497 US NA

**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		WILLIAM BORLAND, JOHN J. FELTEN, Thick Film Ceramic Capacitors and Resistors inside Printed Circuit Boards, 34th International Symposium on Microelectronics (IMAPS), Oct. 9-11th, 2001, Baltimore, MD.	<input type="checkbox"/>
		JOHN FELTEN, RICHARD SNOGREN, JIMING ZHOU, Embedded Ceramic Resistors and Capacitors in PWB: Process and Performance, Fall IPC Meeting, October 11, 2001, Orlando, FL.	<input type="checkbox"/>
		WILLIAM J. BORLAND AND SAUL FERGUSON, Embedded Passive Components in Printed Wiring Boards, a Technology Review, To be published in CircuiTree Magazine, 2001.	<input type="checkbox"/>
		JIMING ZHOU, JOHN D. MYERS AND JOHN J. FELTEN, Embedded Passives Technology for PCBs: Materials, Design, and Process, IMAPS 2002 Conference, Denver, CO, Sept. 4-6, 2002.	<input type="checkbox"/>
		JOHN J. FELTEN, Electronic Circuits World Convention, Paper number IPC31, Advanced Embedded Passives Technologies - Putting Ceramic Components into Organic PWBs.	<input type="checkbox"/>
		WILLIAM BORLAND, JOHN J. FELTEN, SAUL FERGUSON, ALTON B. JONES AND ANGELA A. LAWRENCE, Embedded Singulated Ceramic Passives in Printed Wiring Boards, IMAPS Advanced Technology Workshop on Passive Integration, Ogunquit, ME, June 19-21, 2002.	<input type="checkbox"/>

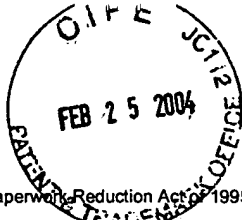
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Attorney Docket Number	EL0497 US NA

Sheet 4 of 4

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		DR. KIM FJELDSTED AND STACEY L. CHASE, EMBEDDED PASSIVES: LASER TRIMMED RESISTORS, CIRCUITREE, Volume 70, March 2002.	<input type="checkbox"/>
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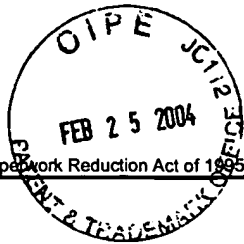
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10/725,888

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